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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,835	10/11/2001	Hiroshi Koshiba	6920/0J924	2278

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,835	KOSHIBA, HIROSHI	
	Examiner	Art Unit	
	John P. Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005 and 04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *2-4,6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the applicant's amendment dated 3/3/2005, and RCE dated 4/4/2005.

The applicant has amended Claims 1-8.

The applicant has added Claims 9-10 as new claims.

Claims 1-10 are pending in this action.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/3/2005 has been entered.

Response to Amendment

2. In view of the applicant's revised drawing FIG.1, the examiner withdraws the objection to said drawing, and approves said figure.

3. In view of the applicant's amendment to Claim 8, the examiner withdraws the rejection of said claim under 35 USC § 112 second paragraph.

4. The examiner maintains the objection to the Disclosure in the first office action because the applicant was non-responsive to this objection.

Response to Arguments

5. Applicant's arguments with respect to the rejection of claims 1-8 under 35 USC § 102 and § 103 have been considered but are moot in view of the new grounds of rejection (see below).

Claim Objections

6. Claims 2-4 are objected to because of the following informalities: The examiner requests that the first line of the claim be changed to; "[A] The semiconductor test apparatus...".

7. Claims 6-8 are objected to because of the following informalities: The examiner requests that the first line of the claim be changed to; "[A] The control method for ...".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art in FIG.4 and FIG.5, and pages 1-5 of the Specification (herein "APA"), and further in view of Enoki et al., U.S. Patent No. 5873085.

As per Claim 1:

The APA teaches a semiconductor test apparatus that tests the operation of a semiconductor based on a plurality of pattern data (page 1 lines 5-10), comprising: a control unit for controlling the semiconductor test apparatus (FIG.4 40); a disc apparatus

(FIG.4 42) and a buffer memory (FIG.4 43) for storing a plurality of pattern files transferred from an external memory (page 1 lines 21-25); an executive memory (FIG.4) comprising a pattern memory (FIG.4 44), an MIC memory (FIG.4 45), and an SPG (serial pattern generator) memory (FIG.4 46) for executing tests for each type of semiconductor by applying test patterns and control data in the executive memories (page 2), but fails to distinctly specify a pattern use frequency table. But in an analogous art, Enoki et al. teaches; a counting device (FIG.34 3107) that counts the number of times the data is used for each of said pattern data files (FIG.34 3106 "ACCESS COUNT"); and a control unit (FIG.34 3109) producing a pattern file use frequency count table (FIG.34 3106) showing the relationship between each of said files and said number of times the files are used (FIG.34 File ID vs Access Count), and storing this pattern file use frequency count table in a pattern file use frequency count table memory (FIG.34 3110). The applicant has not definitely further defined the memory, and so the examiner has equated the disc storage to a memory. The storage system 3110 of FIG.34, depicted in the examiner's reference as a disc storage device, is a well known alternative to a memory, and thus is compatible with "memory" when the storage device is not more definitely defined (as in "DRAM" memory). And Enoki et al., in column 3 lines 1-4 cites the advantage as an improvement in data processing capabilities resulting in the using of the features of this invention. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include features of Enoki et al., such as the data usage table and counting/control unit in

place of the same in the APA in order to more efficiently process the data used in testing.

As per Claim 2:

The teachings of the APA and Enoki et al. further teach the semiconductor test apparatus according to claim 1 wherein said counting device counts the number of times said pattern data is used in a set of test for a predetermined number of semiconductors (FIG.34 3107). The applicant is reminded that the claimed invention must result in a structural difference from the reference in order to patentably distinguish the claimed invention from the prior art. In other words, if the prior art references are capable of performing the intended use, then the prior art meets the claim. In this claim, there is no other apparatus required to meet the requirements of this claim, and in view of the motivation previously stated, the claim is rejected.

As per Claim 3:

The APA and Enoki et al. teach the semiconductor test according to claim 1, wherein said control unit rearranges the pattern files in descending order of frequency of use based on said pattern file use frequency table after producing said pattern file use frequency table (FIG.34 3106). There is no other apparatus required to meet the requirements of this claim, and in view of the motivation previously stated, the claim is rejected.

As per Claim 4:

The APA and Enoki et al. teach the semiconductor test apparatus according to claim 1, wherein said control unit deletes the pattern files in ascending order of

frequency of use in the case that the capacity of the executive memory is insufficient when transferring said pattern files to the executive memories (FIG.4 EXECUTIVE MEMORY). There is no other apparatus required to meet the requirements of this claim, and in view of the motivation previously stated, the claim is rejected.

As per Claim 5:

The APA teaches a control method for a semiconductor test apparatus comprising a disc apparatus (FIG.4 42), a buffer memory (FIG.4 43), and an executive memory comprising a pattern memory (FIG.4 44), an MIC memory (FIG.4 45), and an SPG memory (FIG.4 46), for testing the operation of a semiconductor based on a plurality of pattern data (page 2), but fails to teach the steps of: counting the number of times said pattern data is used for each pattern file; and preparing a pattern file use frequency count table that shows the relationship between each file and each use frequency count corresponding to the number of times each file is used, and storing the pattern file use frequency count table in a memory. But the analogous art of Enoki et al. does teach the same features wherein; a counting device (FIG.34 3107) counts the number of times the data is used for each of the data files (FIG.34 3106 "ACCESS COUNT"); and a control unit (FIG.34 3109) producing a pattern file use frequency count table (FIG.34 3106) showing the relationship between each of said files and said number of times the files are used (FIG.34 File ID vs Access Count), and storing this pattern file use frequency count table in a pattern file use frequency count table memory (FIG.34 3110). The applicant has not definitely further defined the memory, and so the examiner has equated the disc storage to a memory. The storage system 3110 of

FIG.34, depicted in the examiner's reference as a disc storage device, is a well known alternative to a memory, and thus is compatible with "memory" when the storage device is not more definitely defined (as in "DRAM" memory). And in view of the motivation previously stated, the claim is rejected.

As per Claim 6:

The method of Claim 5 is limited to counting the data accesses during a number of semiconductors tested. In the analogous art, Enoki et al. also counts the number of accesses to the system (column 3 lines 44-51), and in view of the motivation previously stated, the claim is rejected.

As per Claim 7:

This claim further limits the method of Claim 5 wherein storing the file is done in descending order of frequency. The Enoki et al. reference discloses this feature in FIG. 38(A). And in view of the motivation previously stated, the claim is rejected.

As per Claim 8:

The APA further teaches the control method of the semiconductor test apparatus according to claim 5, wherein said storage step deletes the pattern in ascending order of frequency of use (FIG.5 5B) in the case that the capacity of the executive memory is insufficient (FIG.5 56) when transferring said pattern files (FIG.5 55) to the executive memories (FIG.4 46, 45, 44). And in view of the motivation previously stated, the claim is rejected.

As per Claim 9:

The APA teaches a semiconductor test apparatus (page 1 lines 21-22) comprising: a control unit (FIG.4 40) for controlling a plurality of memories for executing tests for a plurality of types of semiconductors (page 2); a disc apparatus (FIG.4 42) for storing a plurality of test pattern files for testing a plurality of semiconductors when test patterns are transferred from an external memory (page 2); a buffer memory (FIG.4 43) for storing a plurality of test patterns to be tested when the control unit transfers test patterns from the disc apparatus to executing memories comprising a pattern memory (FIG.4 44), an MIC memory (FIG.4 45), and an SPG memory (FIG.4 46), wherein said pattern memory stores test pattern data for the rest of a semiconductor (page 2 lines 20-24); said MIC memory stores control data that control operations of the semiconductor test apparatus (page 2 lines 20-24); said SPG (Serial Pattern Generator) memory for storing pattern data and for sending the pattern of a periodic clock to a terminal of a semiconductor (page 2 lines 20-24), but fails to teach the pattern file use table. But the analogous art of Enoki et al. teaches; a file use count memory (FIG.34 3110) for storing a file use frequency count table (FIG.34 3106) that shows the relationship between each pattern file and a use frequency count corresponding to the number of times these files are used (FIG.34 3106, File ID and Access Count), and storing this pattern file use frequency count table in the file use frequency count table memory (FIG.34 3110). The applicant has not definitely further defined the memory, and so the examiner has equated disc storage to a memory. The storage system 3110 of FIG.34, depicted in the examiner's reference as a disc storage device, is a well known alternative to a memory, and thus is compatible with "memory" when the storage device

is not more definitely defined (as in "DRAM" memory). And in view of the motivation previously stated, the claim is rejected.

As per Claim 10:

The APA teaches a control method for a semiconductor test apparatus that is executed by a control unit for carrying out test performance of a semiconductor based on a plurality of pattern data (page 3 lines 7-9), comprising the steps of: storing a plurality of pattern data files corresponding to the test items for each type of semiconductor in a disc apparatus (page 1 lines 21-25) and a buffer memory (page 2 lines 1-5); distributing to an executive memory comprising a pattern memory (FIG.5 55), an MIC memory (FIG.5 57), and an SPG memory (FIG.5 59), a pattern data file used in the test for a semiconductor and control data that controls the test from the test patterns (page 2 lines 16-24) after initializing each executive memory (page 4 lines 16-20); carrying out tests of semiconductors in accordance with the pattern data file (page 4 lines 13-15); and deleting a pattern data file from the pattern memory which is the smallest use frequency count in the pattern file use frequency count data table (FIG.5 5B) in the case where the capacity of the executive memory is insufficient when transferring said pattern data files to the executive memory (FIG.5 56, 58, 5A). But the APA fails to teach the frequency use table. But in the analogous art of Enoki et al., the following is disclosed; counting the number of times said data is used for each file as a use frequency count of a data file (FIG.34 3107 under control of 3109); preparing a data use frequency table that shows the relationship between each file and a use count corresponding to the number of times these files are used (FIG.34 3106); storing the file

use frequency count table in a pattern file use frequency count table memory (FIG.34 3110). The applicant has not definitely further defined the memory, and so the examiner has equated disc storage to a memory. The storage system 3110 of FIG.34, depicted in the examiner's reference as a disc storage device, is a well known alternative to a memory, and thus is compatible with "memory" when the storage device is not more definitely defined (as in "DRAM" memory). And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER

App No.: 09/975,835 Docket No.: 06920/000J924-US0
Inventor: Hiroshi Koshiba
Title: SEMICONDUCTOR TEST APPARATUS AND CONTROL METHOD THEREFOR
ANNOTATED SHEET
Sheet 1 of 1

Drawing approved
5/25/05

Fig. 1